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ABSTRACT

Photoluminescence (PL) characterization of 1.3 μm InGaAsP-InP channelled substrate (CS) buried heterostructure laser wafers is reported. The PL of the active region is excited by a CW YAG laser. Laser chips with high threshold or low efficiency are correlated with regions of weak or inhomogeneous photoluminescence signal along the channel (active region). A PL signal is observed only above a threshold power (P_{th}) of the YAG pumping laser for both the active region in the channel and outside the channel. The P_{th} for the active region in a channel is always greater than that in the planar region. Experimental results show that the high threshold of some CS lasers is associated with n-InP buffer layer growth on the channel wall. An analysis of the electrical equivalent circuit model is consistent with the above observation. PL characterization of CS laser wafers can be used to identify defects associated with epitaxial growth and thus provide feedback to the crystal growth system.

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MEMORANDUM FOR FILE

I. INTRODUCTION

The purpose of this memorandum is twofold; first, to describe the use of photoluminescence (PL) in the evaluation of InGaAsP channel substrate (CS) laser material, and second, to present our findings for an experiment with a CS laser wafer in which an attempt was made to correlate PL data obtained from initial laser material with the electrical and physical structure (SEM cross section) of the completed laser chips.

Our initial findings indicate that PL can successfully be used to:

1) Identify particular growth defects; and thus, provide rapid feedback to the crystal growth system.

2) Identify poor CS laser material due to the presence of defects which give rise to a weak, or inhomogeneous PL signal along the channel.

PL has been used in the qualitative identification of defects, and the determination of material composition for quite some time.[2,3,4] PL is an established technique for characterizing planar structures and can be used as a quick, nondestructive evaluation procedure for double heterostructure material. The measured PL intensity in this case is sensitive to Broad Area Laser (BAL) threshold current densities, uniformity, and p-n junction placement of wafers.[1]

However, quantitative evaluation of CS material is much more difficult because the active layer is grown in the second epitaxial growth and it is difficult to restrict the exciting laser illumination only to the channel due to its geometry and size (width $\simeq 4\ \mu m$). Recently, Hatch, *et al.*,[5] described a PL system used in the characterization of epitaxial CS laser structures prior to laser fabrication. Our experimental arrangement and evaluation techniques closely follow theirs. They report that spectral and spatial analysis is routinely performed upon wafers and that there is good correlation with device performance. In particular, a number of effects are identified by Hatch, *et al.*, in a series of pictures; to summarize, these include:

1) Lowered PL of the channel due to reduced thickness of the active layer.
2) Reduction of the InP buffer layer growth resulting in active layer discontinuities within the stripe.
3) Variations of stripe width and cracked channels indicating photolithographic problems and/or undercutting of mask during etching.
4) Diffuse dark spots due to pinholes in the growth structure.
5) Good quality laser material showing continuous stripes, few defects, and relatively high PL.

We have examined several CS wafers and observed a similar range of effects and in addition also find:

1) A measurable PL signal exists only above a threshold power P_{th} of the YAG pumping laser for both the channel and the planar region surrounding the channel.

2) The P_{th} for the channel was always greater than the P_{th} for the planar region.

In fact, for many of our CS wafers the P_{th} required to generate PL in the channel is well in excess of 100 W/cm^2 (between 100 and 500 W/cm^2).

Additionally, this paper presents experimental results which demonstrate the importance of not having buffer layer (n-InP) on the side wall of the channel. Low threshold lasers are produced from regions with no buffer layer on the channel as previously suggested.[12] Correlations between PL observations, electrical, and scanning electron microscope studies (SEM) of CS laser wafers is the subject of this report.

II. EXPERIMENTAL

The CSBH lasers have been fabricated by (i) two step LPE[7,8] (ii) one step LPE over a diffused substrate[9] (iii) One step LPE over an implanted substrate[10] and (iv) by a hybrid LPE and VPE process.[11]

The schematic cross section of a CS laser with a diffused substrate is shown in Figure 1. It consists of an S-doped n-InP substrate, an n-InP Sn-doped buffer layer, an unintentionally doped InGaAsP active layer (E_g = 0.95 eV), a p-Cd diffused layer outside of the channel, a p-InP Zn cladding layer, and a Zn doped GaInAs top layer. Further details about the device structure are contained in Ref. 8.

The experimental set-up is illustrated in Figure 2. Radiation (1.06 μm) from a CW ND:YAG laser is partially focussed onto the InP substrate side of the sample. The power density can be changed with a variable attenuator and is usually between 10 to 100 W/cm^2. This is not sufficient to cause heating problems or optical degradation of the active layer.[7,1] PL is collected normal to the wafer and is directed into the spectrometer, or the Vidicon, when an optional mirror is in place. The distance between the Vidicon and the objective is adjusted so as to form a 400 μm × 500 μm image on the TV monitor. A PbS detector, SPEX spectromer, and a lock-in amplifier are employed for spectral analysis. All measurements are made at room temperature to allow comparison with laser performance.

In the future, the sample mount will be equipped with a position detector so that effects observed in PL can be accurately correlated to their position on the wafer. However, for this study, we simply drew a map of the observed effects in PL on the back side of a photograph of the wafer top surface. In this study, the wafer C191 was processed to produce CS lasers with a window above the active stripe on the n-side metallization. The photolithographic mask used for window laser fabrication was designed with chip and row-column numbers. By taking photographs of the wafer before cleaving and separating it is possible to determine the exact position of resulting chips in the original wafer.

II.1 PL Evaluation

The PL is imaged from the substrate side of CS laser wafers. Typical PL images of a CS wafer (C191) are shown in Figure 3. The image quality is much sharper than the photographs indicate; the graininess is not present on the TV monitor. In fact, one can often discern in PL features that are observed under optical inspection, such as terracing of the active layer. In some cases PL can replace or extend microscopic examination. Figure 3a shows a nonradiative center directly above the channel, which is not expected to affect laser performance. Two bright stripes are seen on either side of the channel. We have observed this in all the CS wafers examined, and it is presumably due to a build-up of active layer which forms at the shoulder of the channel. This is seen in the SEM photographs shown in Figure 4.

A map of the PL features is drawn as each channel is scanned and viewed on the TV monitor. This map is shown in Figure 5. Two top surface In droplets are shown and are used to orient the wafer. Three nonradiative centers (~100-200 μm in diameter) which cross the channel are also noted.

As previously mentioned, a threshold PL was observed for both the planar region and the channel. The channel 'lights-up' or 'turns-on' with the onset of PL. An unusual feature of the turn-on was observed in many of the channels of this wafer. The power density required to cause a channel to light up was observed to vary abruptly from channel to channel or even along individual

channels. A power density of 70 W/cm^2 was sufficient to cause most of the channels to light up. However, the power density required to cause a channel to light-up increased to approximately 150 W/cm^2 in sections of some channels. Areas requiring a high power density for the onset of PL are also noted in Figure 5. This region is directly across from a large In droplet on the top surface, and hence changes in the PL intensity within the channel may be related to compositional changes.

On the whole, C191 is classified as a good wafer by the PL evaluation because, as Figure 3 reveals, the channels are straight, the active region both inside and outside the channel is homogeneous, the PL intensity is uniform (excluding the exception just noted), and the wafer is free of the sorts of defects listed in the introduction.

II.2 Laser Characterization

Wafer C191 was then processed into laser chips. The resulting chips were sorted by cosmetic appearance. An initial lot of 46 unbonded chips that passed cosmetic inspection were tested. All the chips from this initial batch lased; however, the median threshold current (37 mA) was somewhat high. The threshold currents were in the range 39 ± 12 mA.

The measured results on laser chips are presented in Figure 6. The threshold current and dL/dI characteristics are displayed in a small rectangle which corresponds to the chip's position on the wafer. The row and column numbers of the matrix are identical to the window laser ID located on each chip.

A number of not unexpected qualitative remarks can be made about Figure 6. For the most part, chips with similar thresholds come from the same area. The electrical properties of a processed wafer are, on the average, dependent on the chip's position on the wafer. Also, this data lends credibility to the belief that the best chips come from the center of the wafer.

The PL evaluation correctly predicted that lasers made from C191 lased. However, there is no overwhelming similarity between the PL threshold map (Figure 5) and the electrical characterization map (Figure 6), although the data across rows 19, 20, and 21 is suggestive. The

right sides of these rows all show lower threshold currents than the left sides while these same regions in the PL map all possess a higher PL turn-on.

Another feature of interest found in rows 19, 20, and 21 is a cluster of 5 chips (between columns 36-39) all with thresholds less than 25 mA. A number of chips were inspected by SEM in order to determine what sets this low threshold region apart from the rest of the wafer.

II.3 SEM Data

Eleven chips were examined by SEM. Six of these chips were from row 20 since a detailed inspection of this row could provide insight into the change in threshold current across this channel as well as the sudden change in turn-on observed in PL. Initial inspection of the SEM photographs showed no obvious trends — one might expect, for example, a change in the active layer thickness — with the exception of the buffer layer thickness.

The buffer is measured in the planar section and is the lighter region which lies just beneath the planar active material in Figure 4. Figure 7 compares the buffer layer thickness and the threshold currents across channel 20. The trend is clear enough — thin buffer layers, low threshold currents.

Figure 8 is a scatter plot of threshold current vs. buffer layer thickness for all the devices examined. Again, it is found that the lowest thresholds come from the devices with the thinnest buffer layers.

In fact, a closer examination of the SEM photographs reveals what is happening. Figure 4b shows a high threshold device. The buffer layer is thick but more importantly a close look at the shoulder on the channel shows that the buffer layer clearly separates the p-diffused region from the top p-InP region in the channel. In contrast, Figure 4a shows a low threshold device with a thin buffer layer. In this case, the p-diffused region correctly meets the top p-InP region — the buffer layer is not on the sides of the channel. Problems associated with high leakage currents due to buffer layer growth within the channel have always been a source of concern. Evidently, our study indicates that the buffer layer thickness measured outside of the channel is a good gauge by which

to measure the amount of buffer layer grown within the channel. An analysis of the equivalent circuit model of a CS laser with a buffer layer on the channel wall is presented next.

III. EQUIVALENT CIRCUIT MODEL

The electrical equivalent circuit model of a CSBH laser has been described previously.[12] It was stated there that growth of n-buffer in the walls of the groove will increase the leakage current, although the circuit was not analyzed near threshold. The schematic cross section of a CSBH laser with and without an n-InP buffer layer on the walls of the channel is shown in Figure 4. The equivalent circuit model is shown in Figure 9. The major difference in the two equivalent circuit models (with and without n-InP buffer) is the presence of the shunting resistor R when the buffer layer covers the whole p-blocking layer. The current path representing this resistor is shown dashed in the Figure 9.

The active region is represented by a forward biased diode in the equivalent circuit. The p-InP cladding layer and n-InP substrate forms the forward biased p-n diode shunt. The n-InP buffer layer, p-InP blocking layer and the n-InP substrate forms the NPN transistor in the field. The p-InP cladding layer, n-InP buffer layer and the p-InP blocking layer form a PNP transistor which together with the previously mentioned NPN transistor can form a thyristor in areas where active layer is missing in the field. However, because of the presence of the active in the field, the thyristor (PNPN) can be modeled as a forward biased diode (similar to the laser diode) with a NPN transistor in series. As mentioned previously, the buffer layer "shorts" the NPN transistor with an "equivalent resistance" R, thus making this path conduct more current at low voltages which increases the leakage current below threshold. Since the value of R is determined by exact layer placement, doping, and thickness of the n-InP buffer, we present the results of the calculation with R as a parameter.

We now estimate the magnitude of R for a 10^{18} cm^{-3} doped n-InP buffer. The room temperature resistivity (R) is $\sim 3 \times 10^{-2}$ ohm-cm assuming a carrier mobility of 2000 $cm^2/Vsec$. For the dashed current path shown in Fig. 9, the total resistance is given by $R = \rho\, d / L t_B$ where t_B

is the thickness of the buffer layer, L is the length of the laser and d is the effective dimension of the region of current flow in the buffer. For $L = 250$ μm, $d \sim 4$ μm and $t_B \sim 0.1$ μm, the calculated R is $\sim 1\ \Omega$.

Figure 10 shows the calculated threshold as a function of $1/R$. The value of R is also shown on the top scale of the abscissa. The results are plotted as a function of $1/R$ (which is proportional to the thickness of the buffer layer) in order to show similarity with the experimental results (Figure 8). The circuit parameters used in the calculation are described in the Appendix.

IV. CONCLUSION

The photoluminescence from the active region of channelled substrate buried heterostructure laser wafers can be used to identify defects associated with epitaxial growth and thus provide pre-processing feedback to the crystal growth. Laser chips with high threshold and low efficiency are correlated with regions of weak or inhomogeneous photoluminescence signal along the channel (active region).

PL examination is useful in optimizing laser yield from CS wafers. However, an accurate prediction of final chip yield is limited by subsequent processing losses and PL's insensitivity to electrical leakage currents in lasers. Currently, a model incorporating lateral spreading of photoexcited carriers, similar to that proposed by Degani, Wilt, and Besomi to explain the suppression of PL signal in double heterostructure wafers, is being explored.[13] It is hoped that a theoretical model can be exploited to provide a quantitative measure of the relative radiative efficiency of CS laser wafers.

Our experimental results show that high threshold currents of some CS lasers are associated with the growth of n-InP buffer layer on the walls of the channel. An analysis of the electrical equivalent circuit model of the CS laser is presented. The results of the analysis are consistent with the above observation.

Acknowledgements

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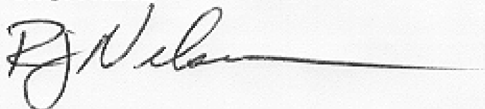

NT
MH-52321-NKD-slc
DPW
RJN

Atts.
Appendix
References
Figure Captions
Figures 1-10
Photo NOs. B83 2278-MH
B83 2279-MH

APPENDIX

The circuit shown in Figure 9 is analyzed using the program SPICE (available on UNIX and Honeywell 600 at Bell Laboratories). The transistor and diode elements in the SPICE program are specified by their saturation parameters (I_s, I_{sd}), ideality factor for the diodes (η) and the forward and reverse current gain for the transistor (BF, BR). These quantities are related to the layer thicknesses and doping levels in the laser structure. The saturation parameter for an ideal diode is

$$I_{sd} = AJ_s$$

with

$$J_s = en_i^2 \left(\frac{D_p}{L_p P} + \frac{D_n}{L_n N} \right) \tag{A1}$$

where A is the area, e is the electron charge, n_i is the intrinsic carrier concentration; D_p, L_p, P are the diffusion constant, diffusion length, and doping of the p-layer, respectively; and D_n, L_n, N that of the n-layer. The transistor parameters are given by

$$I_s = \frac{A_e D_b n_i^2}{N_b L_b}$$

$$\frac{1}{BF} = \left(\cosh \frac{W}{L_b} - 1 \right) + \frac{D_e}{D_b} \frac{L_b}{L_e} \frac{N_b}{N_e} \sinh \frac{W}{L_b} \tag{A2}$$

$$\frac{1}{BR} = \left(\cosh \frac{W}{L_b} - 1 \right) + \frac{D_c}{D_b} \frac{L_b}{L_c} \frac{N_b}{N_c} \sinh \frac{W}{L_b}$$

where D_b, L_b, N_b are the minority carrier diffusion constant, diffusion length, and carrier density in the base; D_e, L_e, N_e that in the emitter; and D_c, L_c, N_c that in the collector, respectively, and W is the base width.

We have assumed that the minority carrier diffusion length and diffusion constant in p-type material are 5 μm and 50 cm²/sec and that in the n-type material are 1 μm and 5 cm²/sec, respectively. The laser length is assumed to be 250 μm.

The parameters used for the active region diode (lasing branch) are $I_{sd} = 3 \times 10^{-11}$ Amp and $\eta = 2$ which corresponds to a threshold current of 7 mA in the absence of any leakage path. For a 0.2 μm × 250 μm active region, this represents a broad area threshold of 1.8 kA/cm^2.

The parameters used for the NPN transistor are $I_s = 7.2 \times 10^{-2}$ Amp, $BF = 26$, $BR = 5$ which corresponds to a base (p layer) thickness of 1 μm and doping 10^{18} cm^{-3}. The collector (n buffer regrown layers) and emitter (n-substrate) dopings are 4×10^{17} cm^{-3} and 10^{18} cm^{-3}, respectively. The parameters for the diode in series with the transistor are $I_{sd} = 7.5 \times 10^{-10}$ Amp and $\eta = 2$. Since this diode is similar to the laser diode, the saturation parameter of this diode is obtained by multiplying the saturation parameter of the laser diode by the ratio of the respective areas. The resistance R_1, R_2, R_s, are assumed to be 1Ω. Figure 9 shows the calculated threshold current as a function of $1/R$.

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FIGURE CAPTIONS

(1) Schematic cross-section of a CS laser chip from wafer C191.

(2) Schematic of the PL experimental set-up.

(3) Photographs of the PL from wafer C191. The channels shown are ~400 μm long and free of defects.

(4) SEM photographs of a low and high threshold laser chip from wafer C191, (scale: 1 mm = 2 μm).

(5) Map of pertinent features observed in PL from wafer C191.

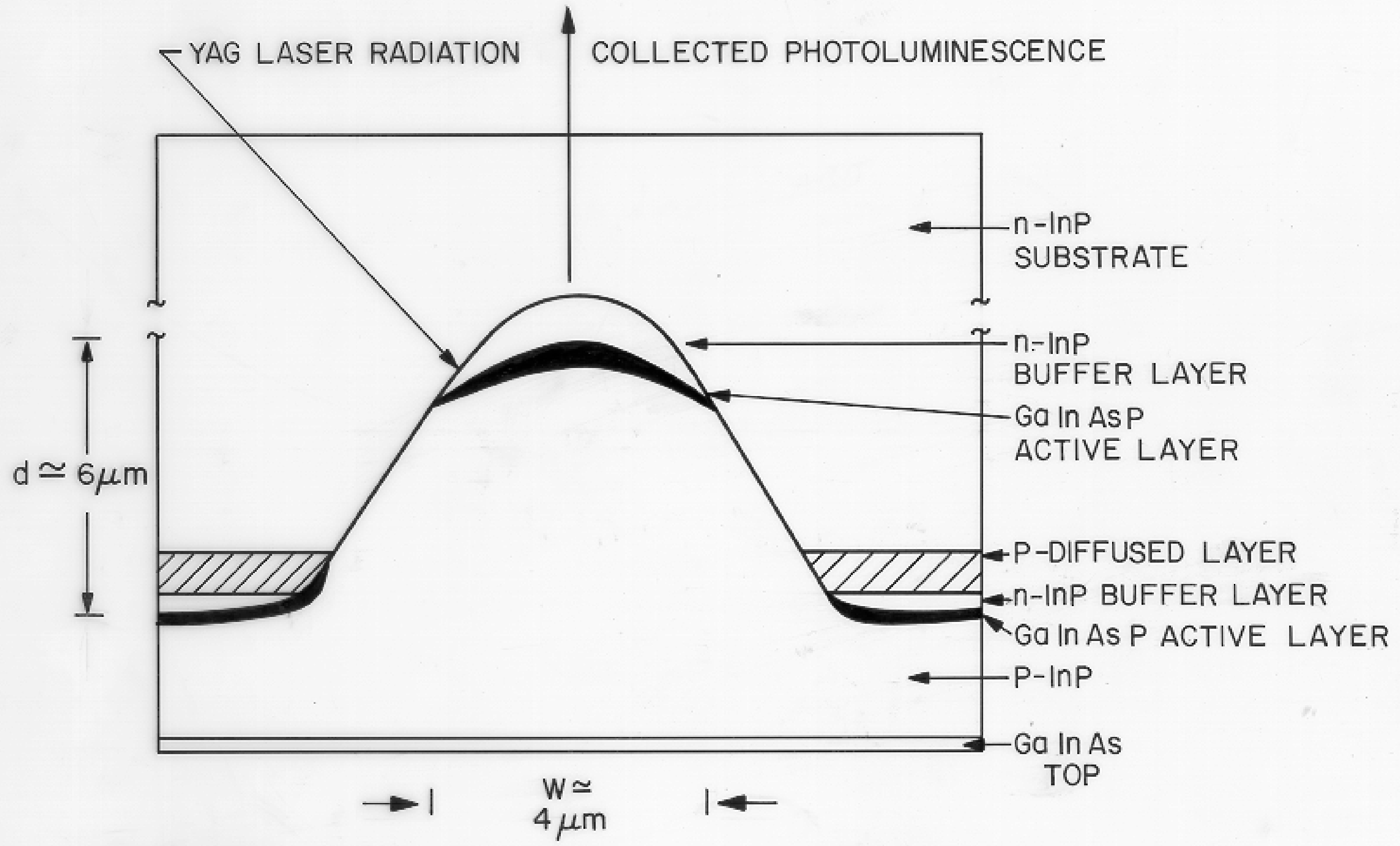
(6) Laser characterization results are shown at their site positions on wafer C191.

(7) Histogram of threshold current and buffer layer thickness across row #20 of wafer C191.

(8) Scatter plot of threshold current vs. buffer layer thickness.

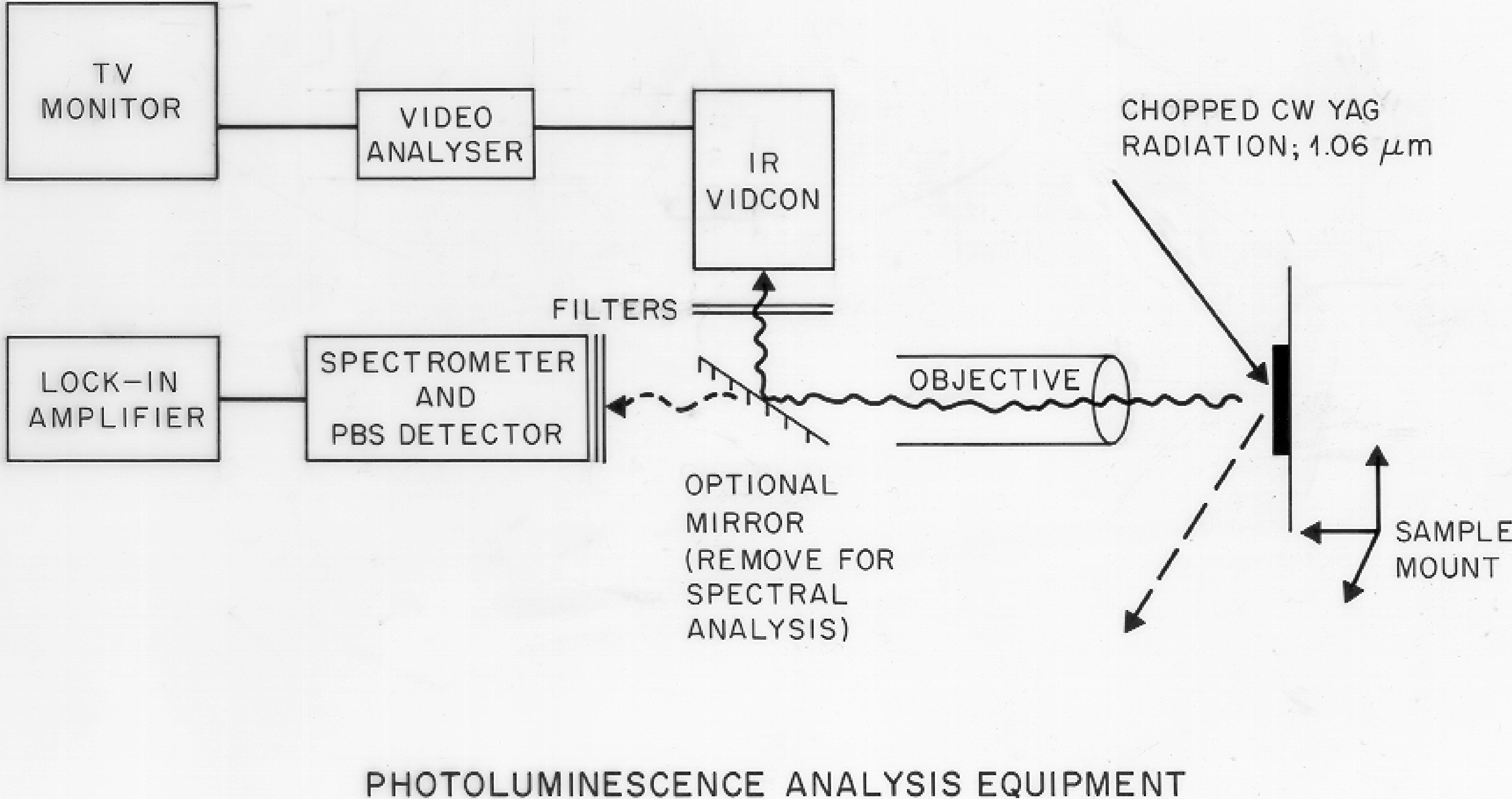
(9) Equivalent circuit models of CSs with and without buffer on the CS wall.

(10) The threshold current as a function of buffer layer thickness ($1/R$) predicted by equivalent circuit model. Compare to Figure 8.



SCHEMATIC CROSS-SECTION OF CHANNEL SUBSTRATE

FIGURE 1



PHOTOLUMINESCENCE ANALYSIS EQUIPMENT

FIGURE 2

Bell Laboratories CASE NO. 11147-0361 NEG NO. B 83 2278-MH

NON-RADIATIVE CENTER

CHANNEL

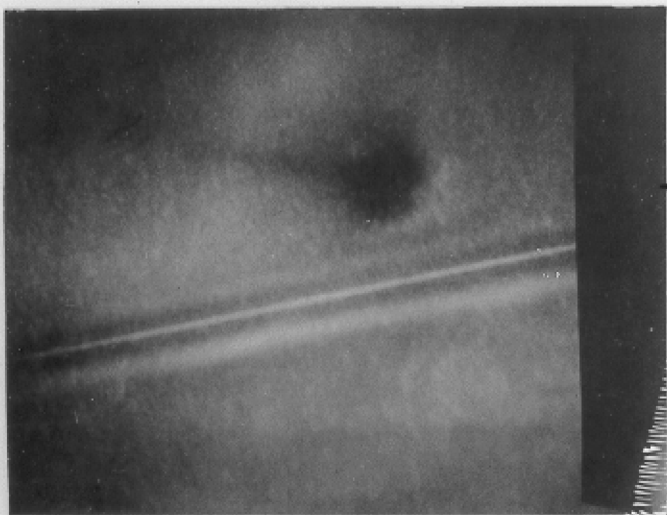


PHOTO 3a

CHANNEL

PHOTO 3b

PL IMAGES

Figure 3.

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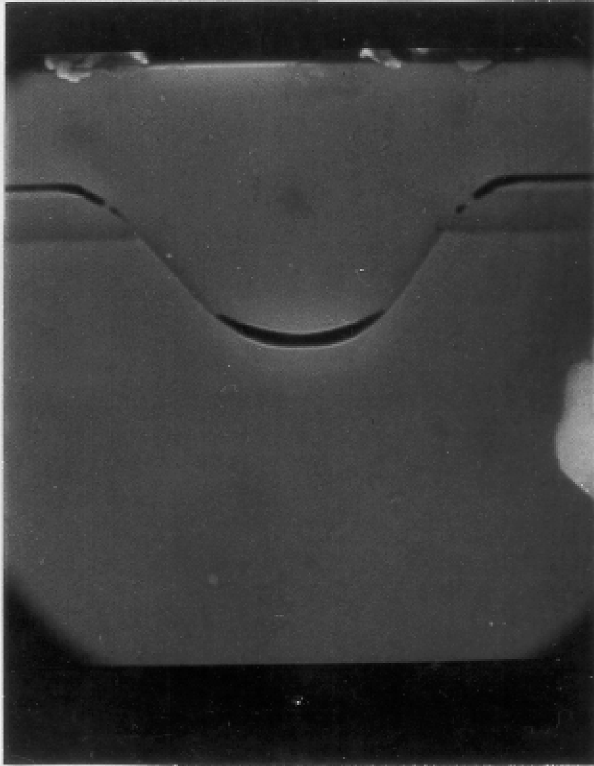
CASE NO. 11147-0361 NEG NO. B 83 2279-MH

BUFFER NOT ON CS WALL

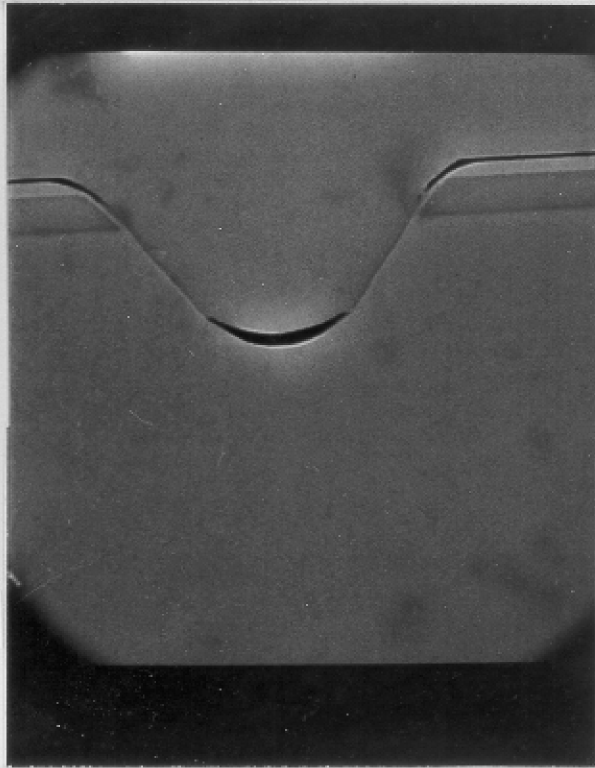


BUFFER THICKNESS

CHANNEL THICKNESS

1mm=2μm

BUFFER ON CS WALL



WINDOW LASER: 40 20

I_{th} = 25mA

B_t ~ .2 μm

PHOTO 4a

WINDOW LASER: 30 19

I_{th} = 72 mA

B_t ~ .4 μm

PHOTO 4b

Figure 4.

In Droplet

NON-RADIATIVE CENTER

HIGH TURN-ON

WINDOW LASER ROW #

26
25
24
23
22
21
20
19
18
17
16

26 28 30 32 34 36 38 40 42 44

CHANNELS

WINDOW LASER COLUMN #

MAP OF FEATURES OBSERVED IN PL

PL MAP C0191

FIGURE 5

3133 1A / wlb / cdi

WINDOW LASER ROW #	26		28		30		32		34		36		38		40		42		44	
26			57 / .1	57 / .08	51 / .09	55 / .09	59 / .09		40 / .12		62 / .08		62 / .08	59 / .09	56 / .1					
25			46 / .13			49 / .13	44 / .13		54 / .11			56 / .1	46 / .14	66 / .1		53 / .1				
24			58 / .8		34 / .11		46 / .15	47	51 / .1		45 / .11		43 / .16	38		37 / .13	36 / .12	61 / .09		
23		47 / .11	51 / .1	52 / .1	38 / .15		43 / .11		39 / .14	37 / .11		29 / .12	35		22 / .13	30 / .13				
22			50				41 / .12	57 / .1		35 / .12	29		25 / .14			37 / .11				
21		23 / .14					46 / .11	32	47 / .12			22			35 / .13	34 / .13	39	35 / .13		
20			51 / .09	48 / .09	44 / .11		41 / .1	33 / .12	26 / .12		25 / .16	25 / .14	23 / .13		25 / .14	27 / .12		30 / .14		
19			54	48 / .1	72	47 / .1	37 / .12	34				24 / .14		33 / .13						
18					53 / .1	57 / .09	49 / .1		27 / .13						58 / .15					
17			55 / .12	53 / .09		59 / .12	45 / .12	64 / .12	48 / .12		48 / .12	54 / .11	42	49 / .12						
16			34 / .13	35 / .12	40 / .1		46 / .1	47 / .11	47 / .1			52 / .12	45 / .1							

ROW # 22 ↓

← THRESHOLD (mA)

← dL/dI

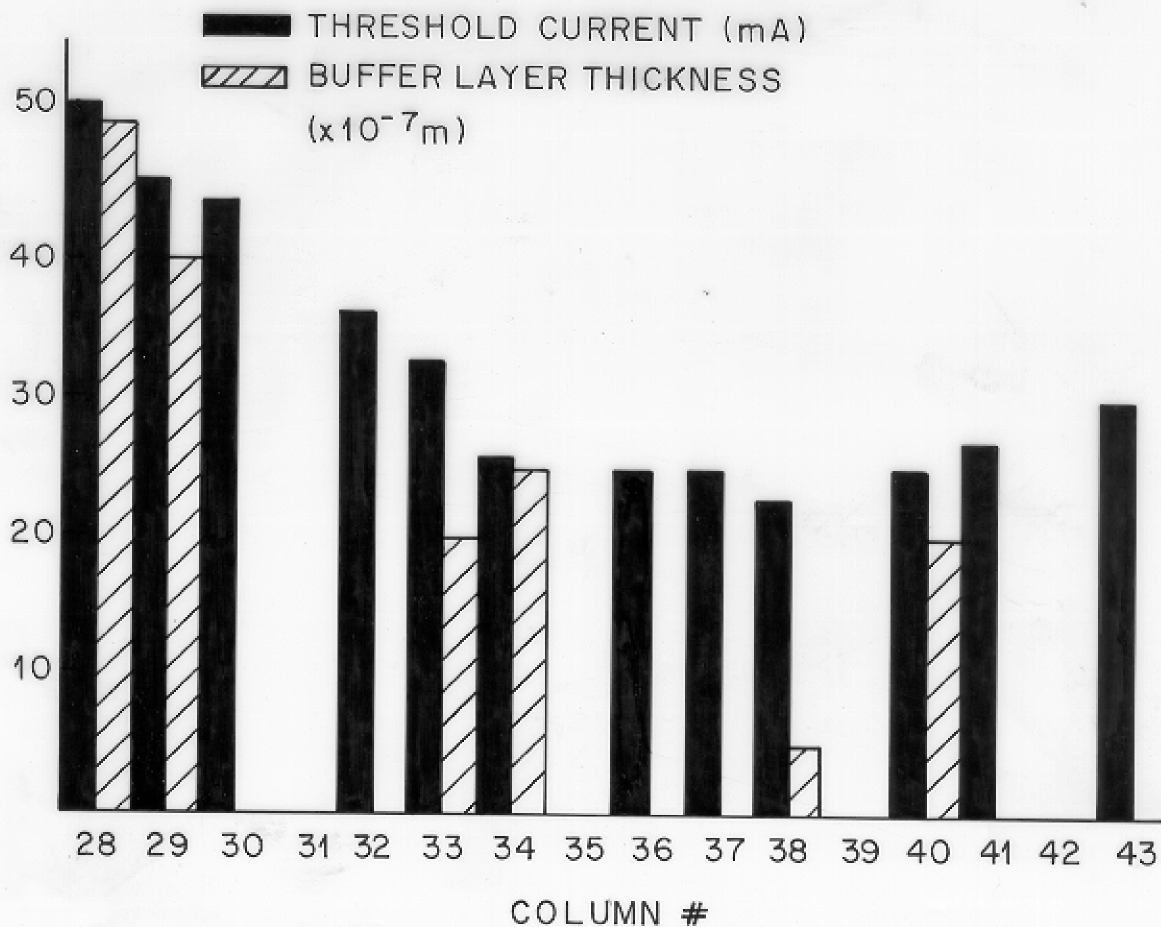
CHANNELS →

WINDOW LASER COLUMN #

LASER THRESHOLD VS. POSITION

FIGURE 6

31331A/wtb/c



THRESHOLD CURRENT AND BUFFER LAYER THICKNESS VS POSITION: ROW # 20

FIGURE 7

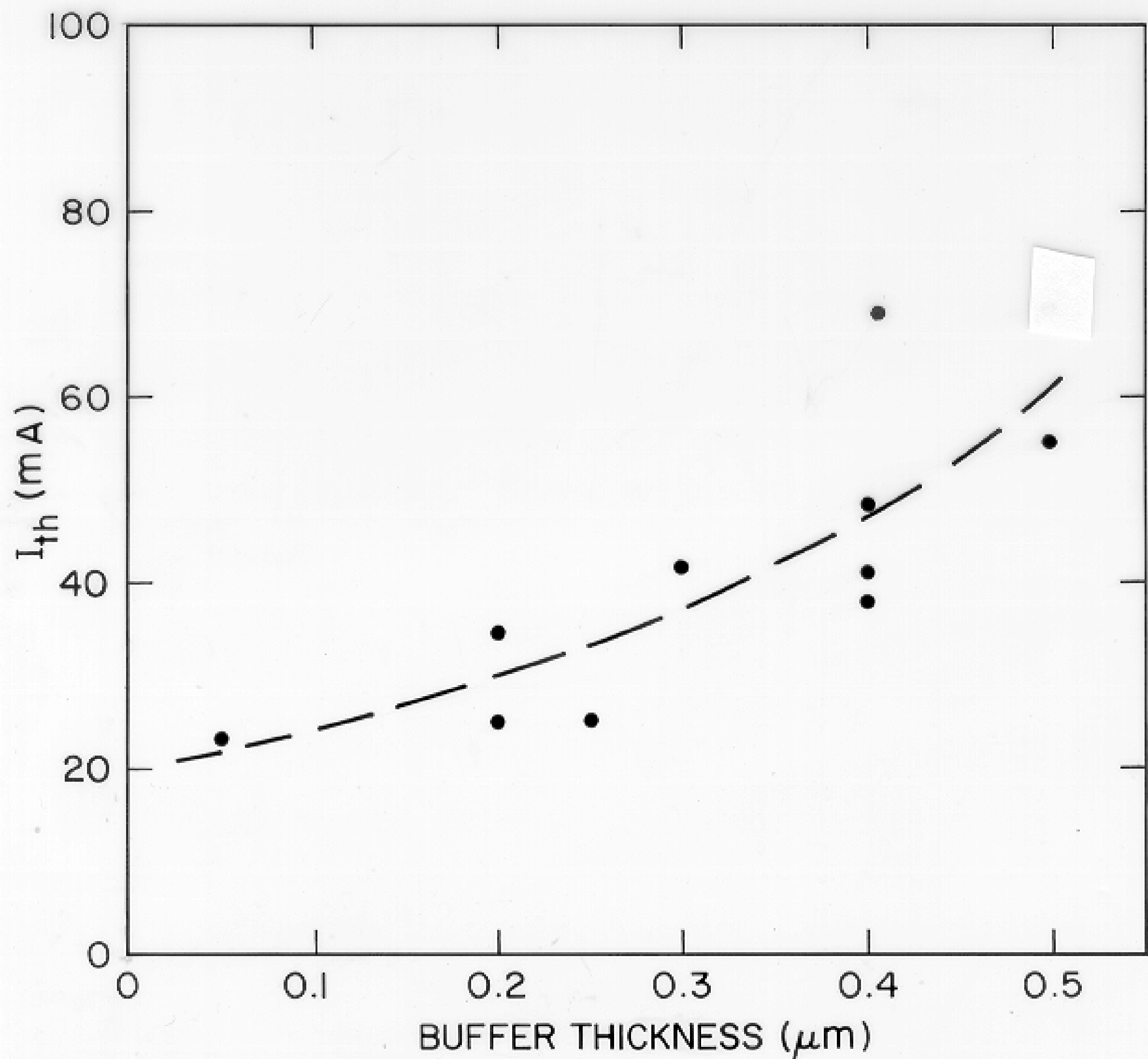


Figure 8.

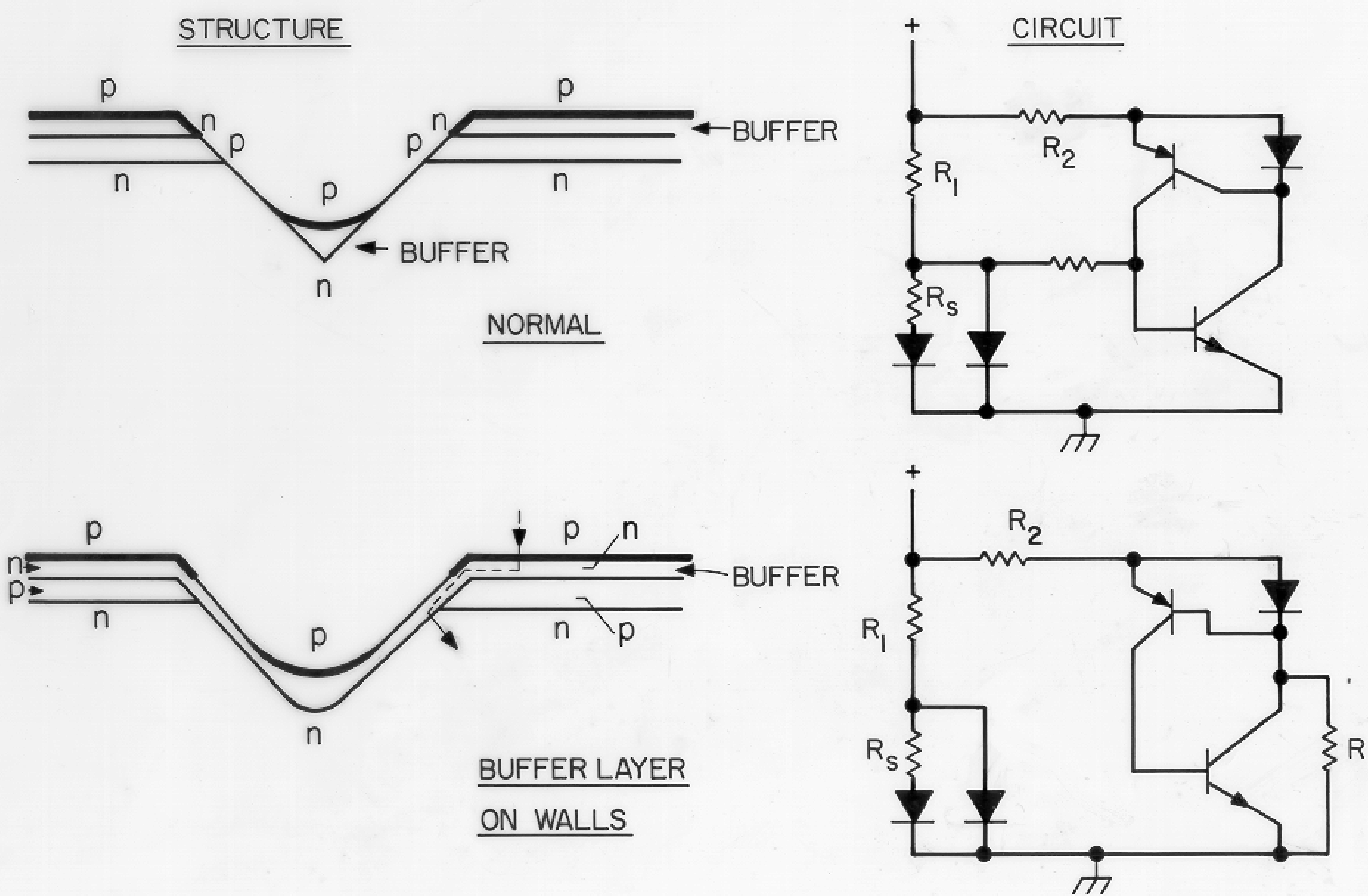


Figure 9.

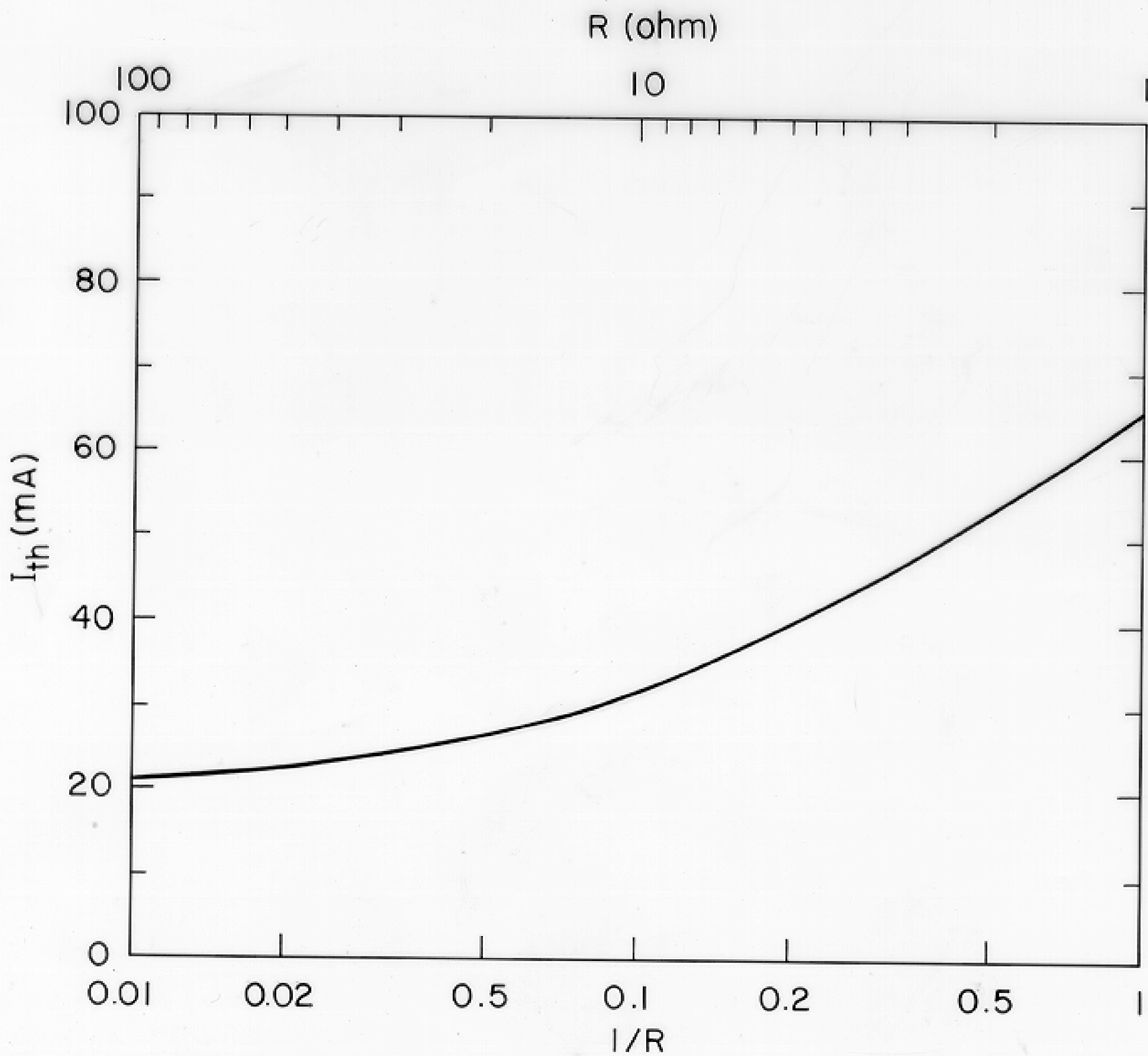


Figure 10.